

---

# **Broadcom Calisto™: A Multi-Channel Multi-Service Communications Platform**

*John Nickolls  
L.J. Madar III  
Scott Johnson  
Viresh Rustagi  
Ken Unger  
Mustafiz Choudhury*

**Broadcom Corporation**

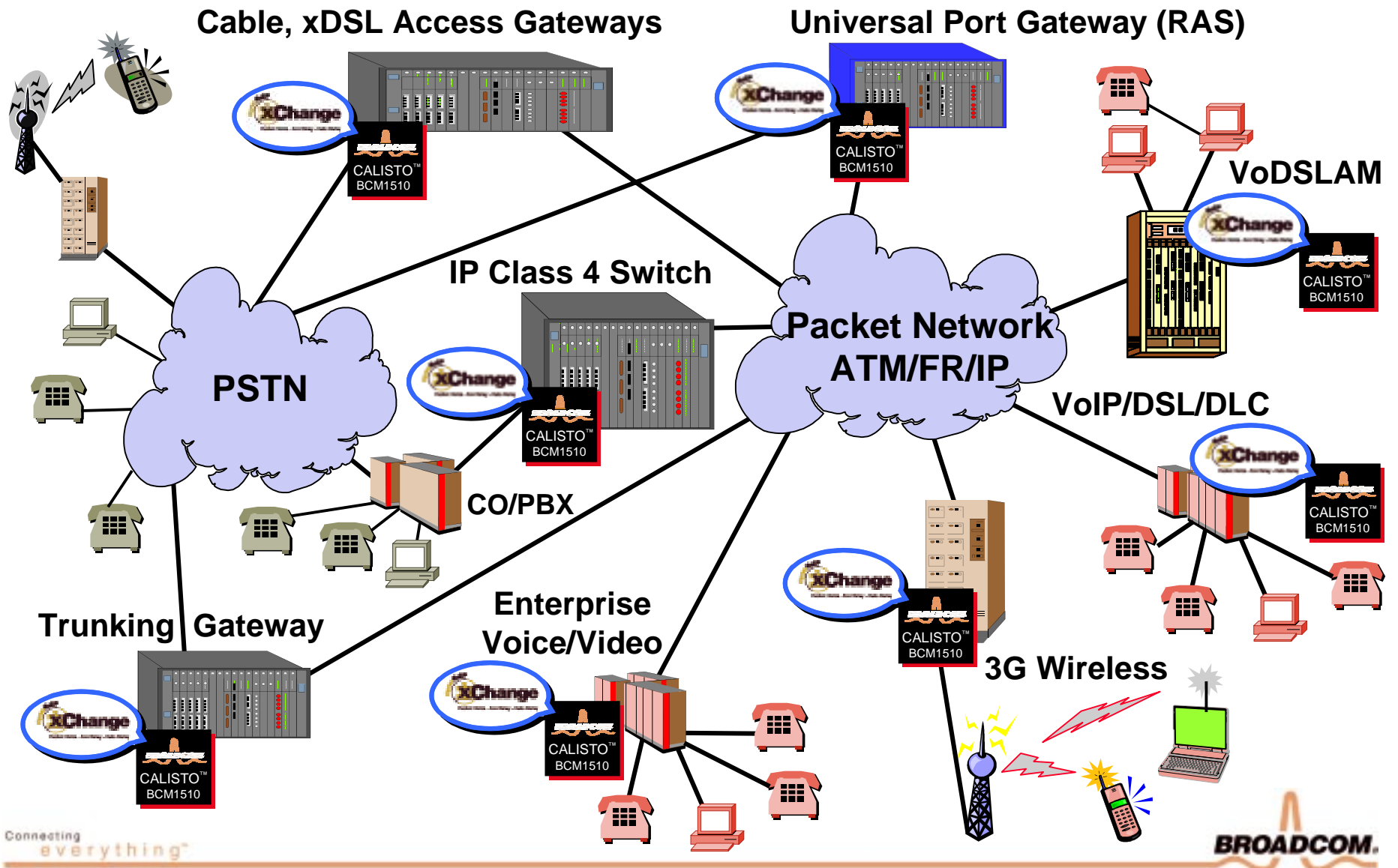
[nickolls@broadcom.com](mailto:nickolls@broadcom.com)

# Calisto™ Outline

---

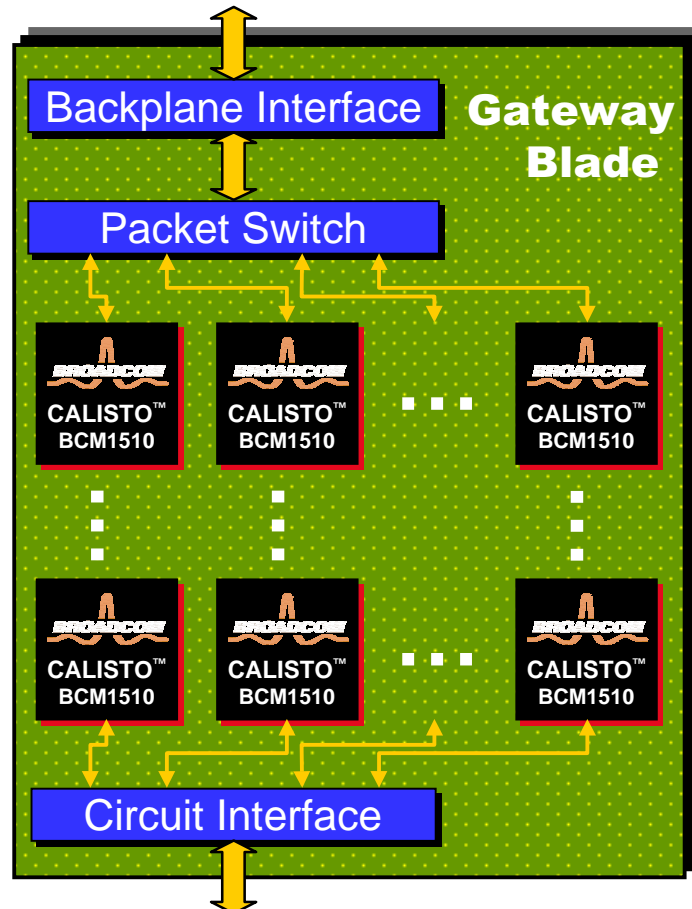
- **Communications gateways**
  - Multi-channel, multi-service, real-time
- **Platform architecture**
  - Cluster architecture
  - SpiceEngine vector DSPs
  - Shared memory
  - Multi-channel I/O
- **Implementation**
- **Performance**
- **Summary**

# Multi-Channel Communications



# Calisto™ Gateway Blade

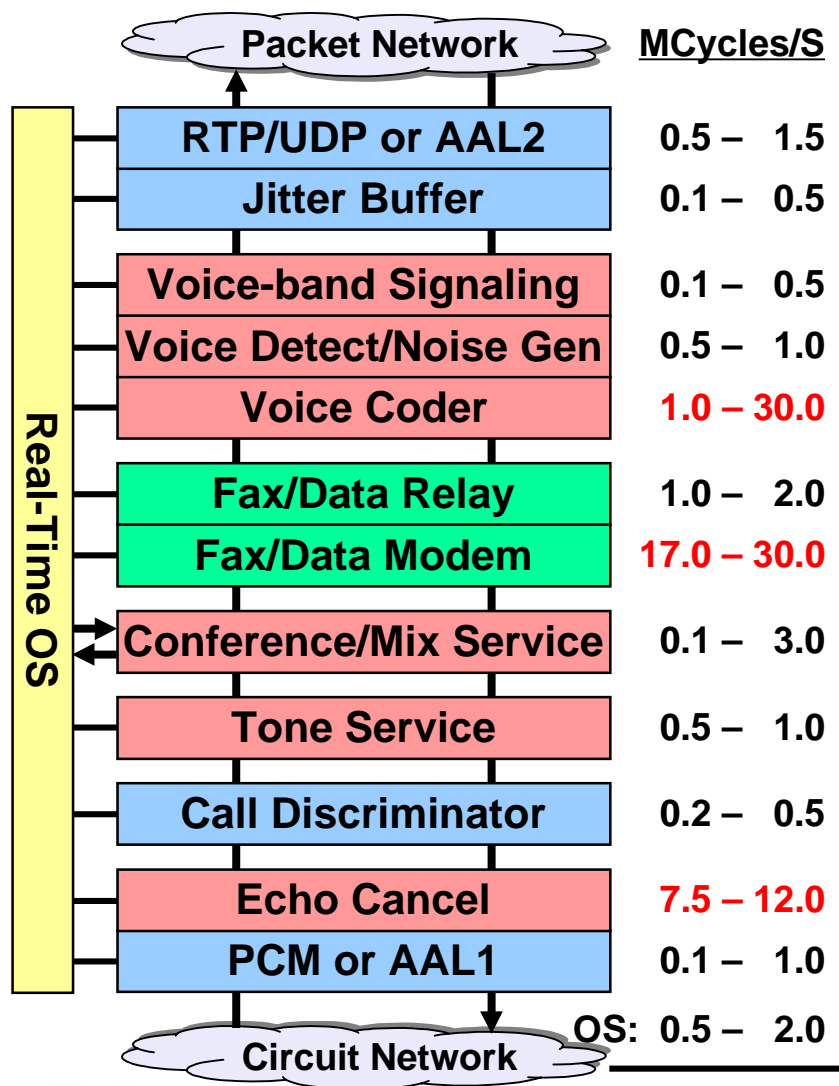
Packet Backplane Interconnect



Circuit Backplane Interconnect

- **Carrier-class/enterprise gateways**
  - Voice over packet, media, fax, data, wireless, trunking, remote access
  - Require many diverse services
  - Require 1000's of channels per blade
  - Severely limited power budget
- **Prior gateways were low density**
  - Complex designs, many different chips
- ➔ **Calisto is a gateway on a chip**
  - Integrates DSPs, CPUs, RAMs, I/O
  - Programmable multi-service platform
  - Supports 60 – 240 channels per chip
- **Simple Calisto chip array**
  - Enables over 2,016 channels per blade
  - ➔ Efficient low-power design

# Multi-Service Gateway Stack

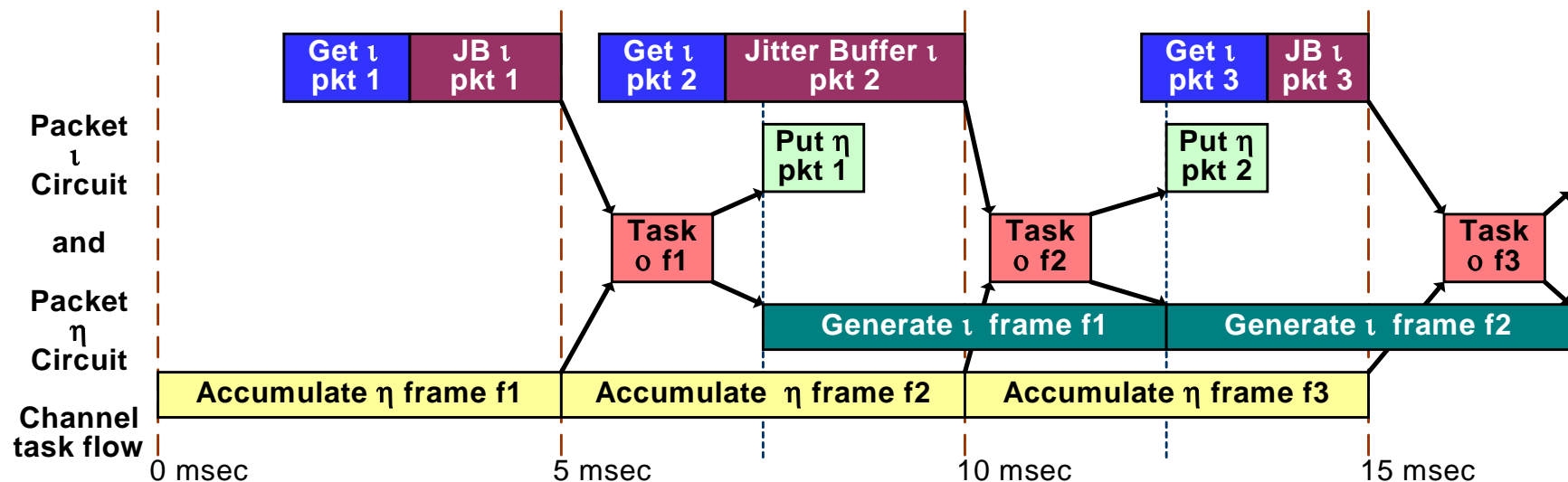


Total: **11 – 53 MCPS** required per channel

- **Complex service suite**
  - Minimize assembler
  - Flexible compiled C software
- **Any service, any port, any time**
  - Total program image 200 – 700 KB
  - Single-image shared memory
- **Compute + memory demand**
  - 11 – 53 DSP/RISC MCPS/channel
  - 4 – 20 KB inter-frame data/channel
  - Balanced compute and memory
- **Mix of DSP, packet, OS work**
  - No time for DSP task + packet task
  - Hybrid DSP/RISC processors
  - Dedicated OS processors

# Many Real-time Periodic Tasks

- **Process frames periodically for all channels**
  - Service-specific frame period: 5, 6, 10, 16.7, 20, or 30 msec
  - 800 to 3,000 tasks/sec per DSP, or 4 to 15 tasks per frame period
  - Every service stack can be executed any time
- **Requires low latency processing delay with low jitter**
  - Incremental latency of 1 – 2 msec, jitter under 250  $\mu$ sec
  - Combine all processing in single per-frame task, minimize overhead



# Mapping Application Attributes

<b>Application Attribute</b>	<b>→ Platform Architecture</b>
Many independent channels	→ Many processors, many parallel per-channel tasks
Many diverse services	→ Programmable, primarily in C; large instruction memory, fast cache fill
High channel density	→ Minimize power, share resources
Digital signal processing	→ Vector data parallelism, operand throughput, memory bandwidth
Network packet processing	→ Task parallelism, sequential protocols
Mix of DSP and packet work	→ Hybrid DSP/RISC processors
Low latency, low jitter	→ Consistent task run time, minimize task overhead and contention

# Calisto BCM1510 Architecture

- Clusters partition functions**

**CM** 1 MB Total Cluster Memory

- Task data, I/O buffers, stacks

**CP** 4 Cluster Processors

- Run OS and supervise cluster

**SE** 16 SpiceEngine DSPs

- Run DSP/packet tasks

**MB** 5 Memory and I/O Bridges

- Share resources efficiently**

**SM** 768 KB Shared Memory

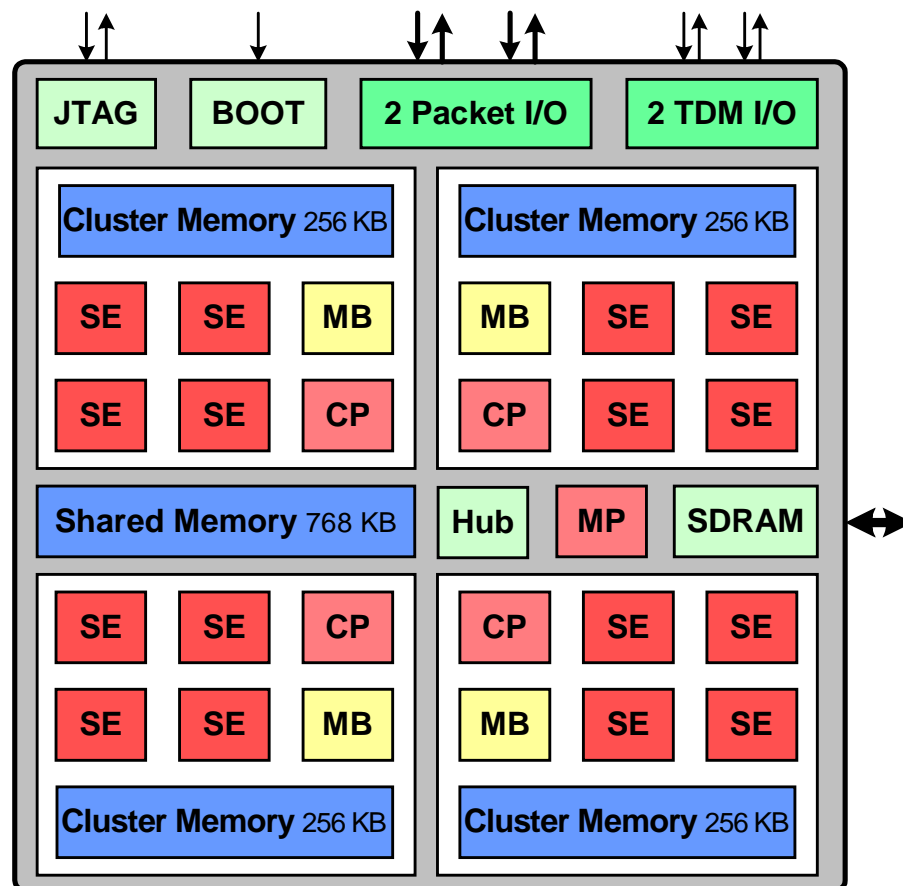
- Single OS & application image

**I/O** 4 Multi-channel I/O interfaces

**MP** Main Processor

- Runs OS and supervises chip

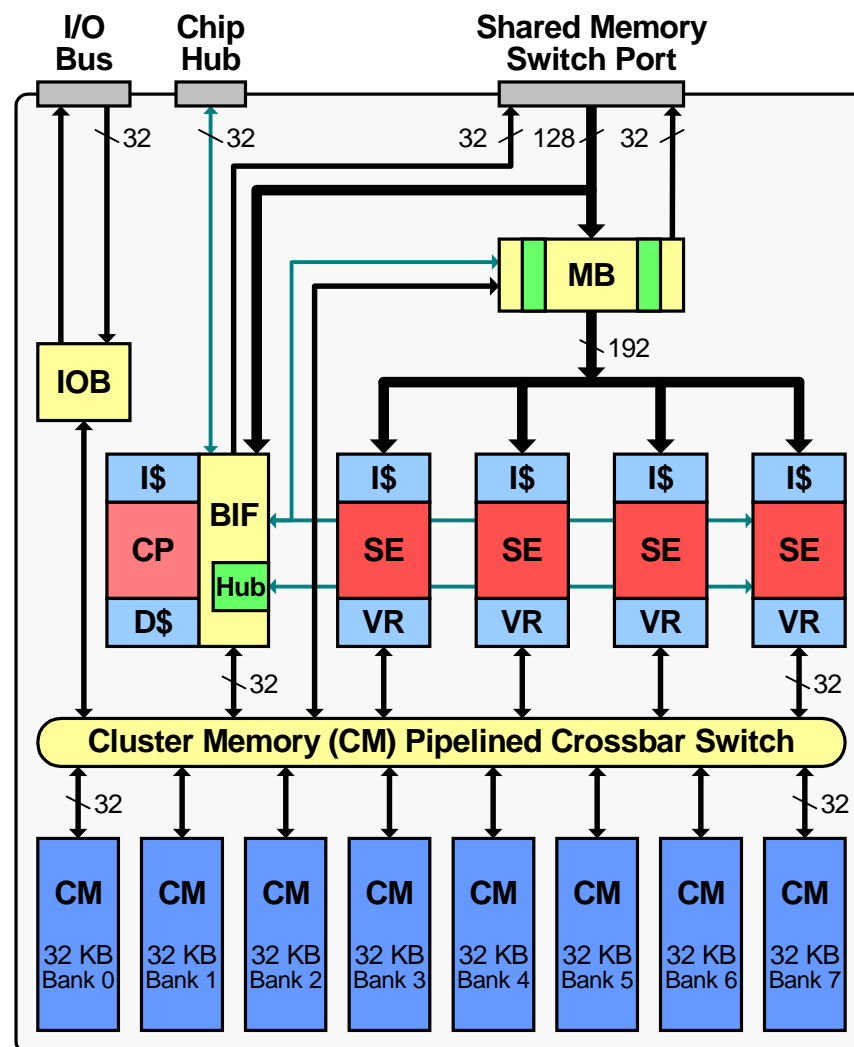
**Hub** Chip synchronization Hub



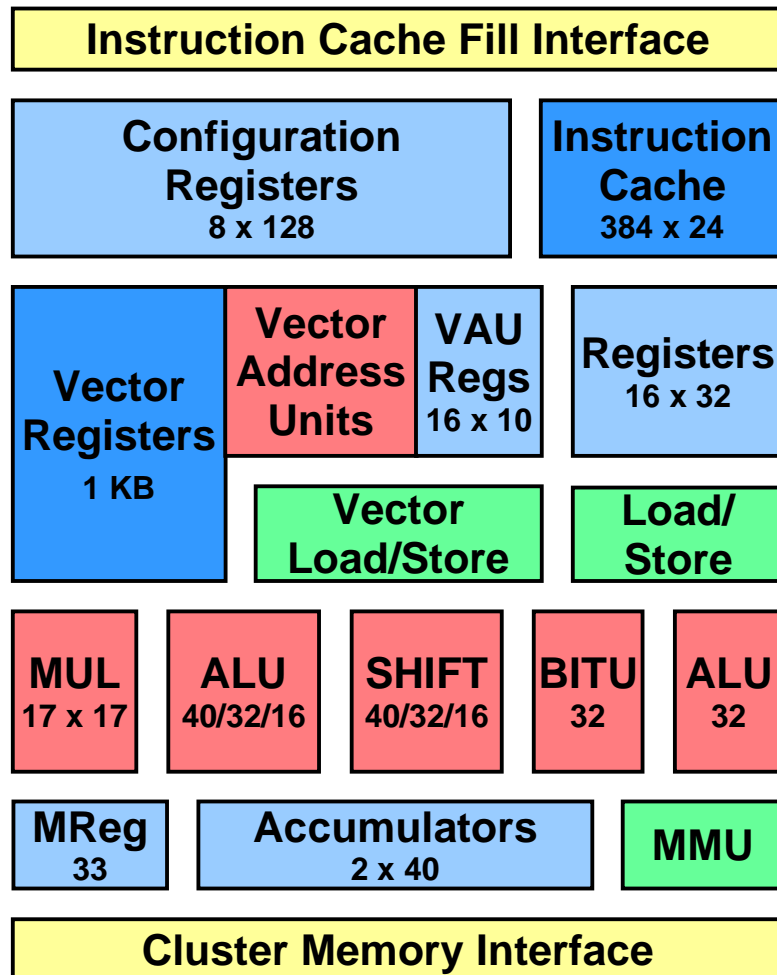


# Cluster Architecture

- **256 KB Cluster Memory** CM
  - Shared by CP, SEs, MB, I/O
  - Task, OS, I/O communication
- **Pipelined CM switch** CM
  - Low latency SE load pipeline
  - Minimal memory contention
- **Cluster synch hub** Hub
- **4 SpiceEngine DSP pool** SE
  - Next available SE runs task
  - No channel affinity → min latency
- **RISC Cluster Processor** CP
  - Schedules SE tasks and output
  - Services interrupts and input
  - Frees SEs of overhead

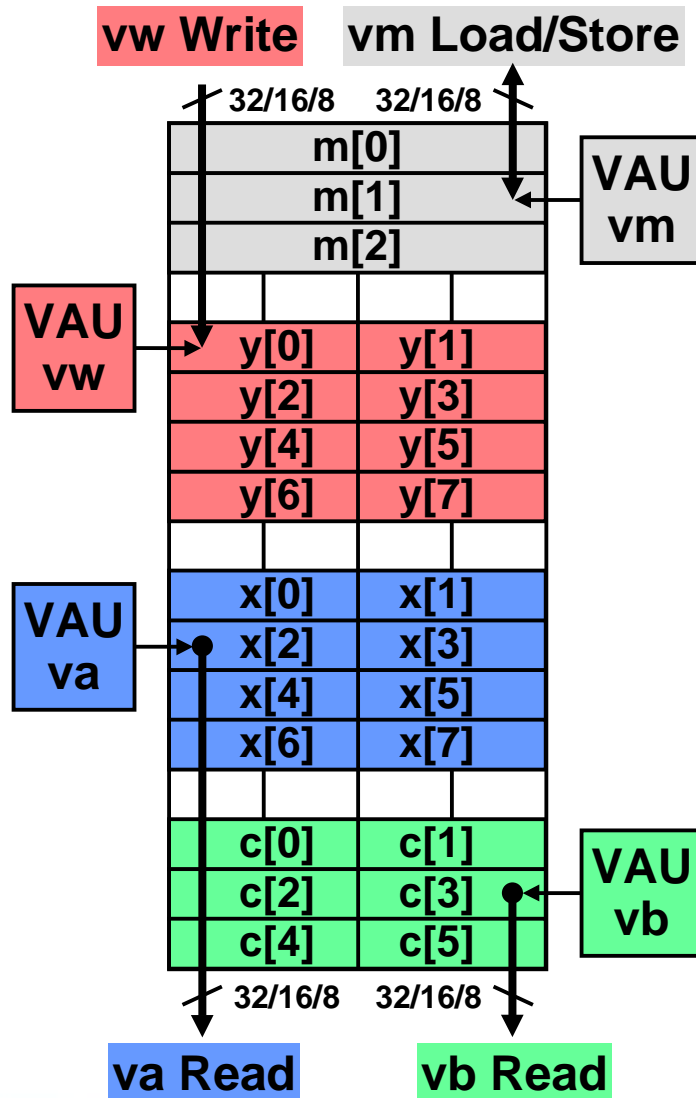


# SpiceEngine™ Vector DSP



- **Vector registers**
  - Fast structured data access
  - Reduce cluster memory demand
- **Fixed-point DSP pipeline**
  - Configurable 16/32/40 bits
  - 10 Parallel operations/cycle
  - ITU saturation arithmetic
- **Efficient C compiler target**
  - Simple single-MAC datapath
  - Narrow 24-bit instruction issue
  - Wide configuration register issue for loops and vector operations
  - Fewer cycles than comparable DSPs, using primarily compiled C

# Why Vector Registers?



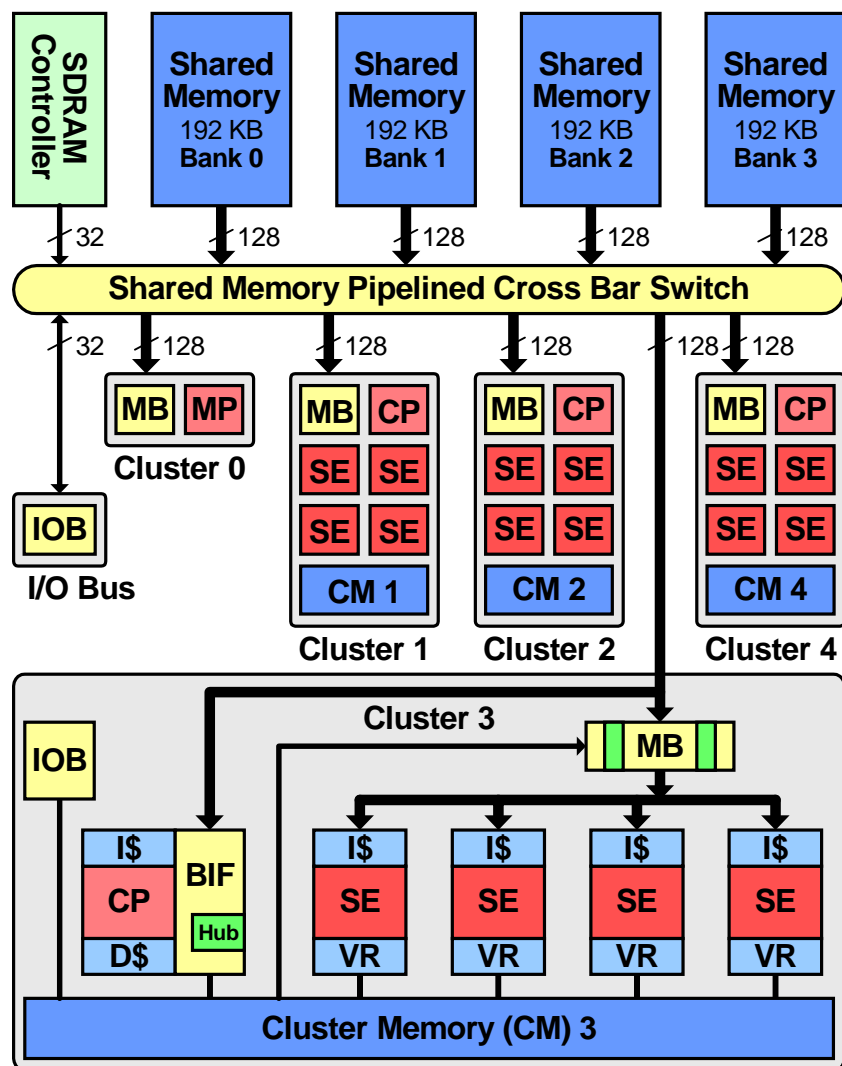
- **Fast structured data access**
  - Vectors, arrays, tables, lists
  - Multi-port vector register access
  - Compiler-scheduled preload
- **Efficient DSP performance**
  - Vector preload covers memory latency, unlike data cache miss
  - Reduce DSP memory accesses and power:  $O(N \cdot T) \rightarrow O(N + T)$
- **Vector address unit (VAU)**
  - Low overhead strided address
- **Vector registers & configurations**
  - Sustain 1 cycle per MAC with minimal memory bandwidth

# Vectorizing C Compiler & Tools

---

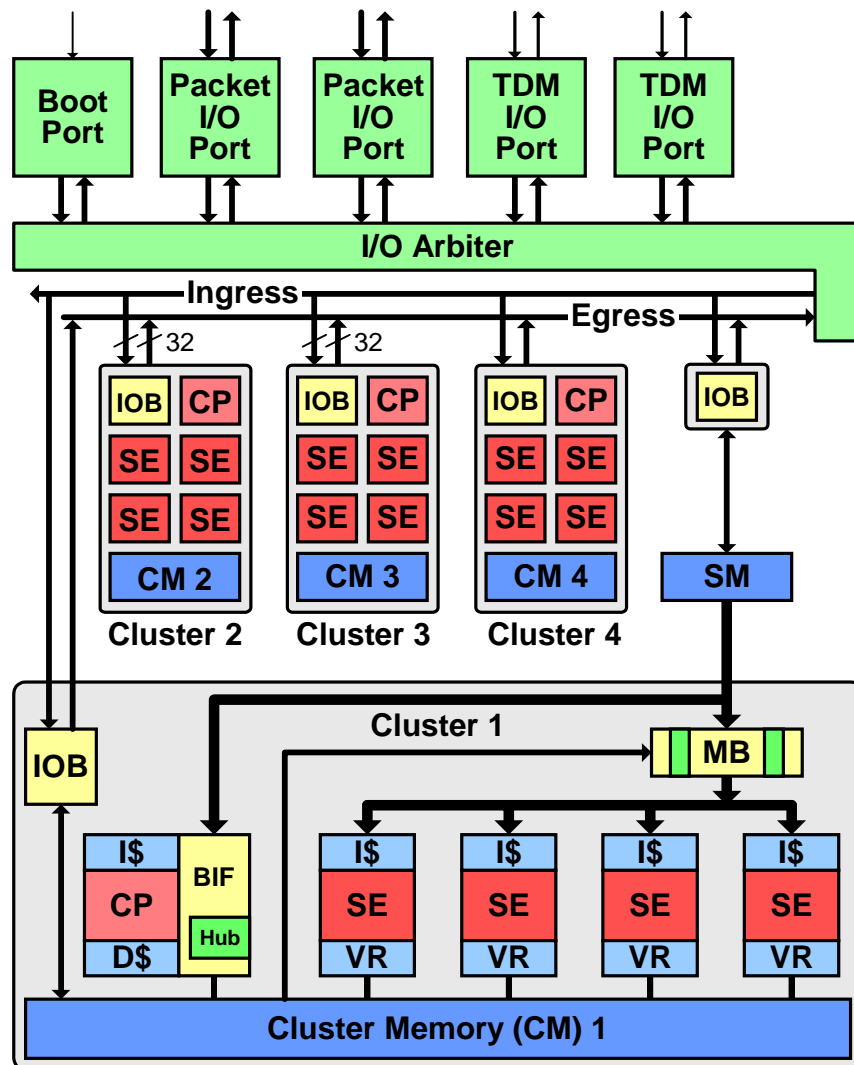
- **Multi-level loop vectorization**
  - Automatic and manual vector register allocation
  - Vector register load scheduling
  - Multi-level vector stride detection
- **Dynamic configuration generation**
  - Minimum-cost configuration generation, load scheduling
- **Signal processing, cross-module optimizations**
  - Value range optimization, saturation algebra
  - Intrinsic deduction, inlining, constant propagation
  - Redundant store elimination (e.g. ITU overflow flag)
- **High-efficiency signal/packet processing in C**
  - Typical ITU reference C within 2x cycles of hand-coded assembler
  - ➔ Enables complete C service stacks, including DSP and network code
  - Multi-channel debugging, profiling, performance tuning tools

# Cache Fill from Shared Memory



- **Shared Memory** SM
  - Single program image, 768 KB
  - Fills SE & CP instruction caches
  - Interleaved 4 banks x 128 bits
- **Pipelined crossbar switch** SM
  - Delivers full 512 bits per cycle
  - Typical utilization 50% – 80%
  - Supports I/O bus and SDRAM
- **SE instruction cache fill** I\$
  - Memory Bridge DMA engine MB
  - Cache reduces memory demand
  - 192 byte line amortizes latency
  - Average miss cost: 0.1 – 0.2 CPI

# Multi-Channel Scatter/Gather I/O



- **Packet and cell network I/O**
  - IP and ATM networks
  - 100 Mbps full duplex, pin-efficient
- **TDM sample stream I/O**
  - Circuit and AAL1 networks
  - Bit-serial ports
- **Multi-channel scatter/gather**
  - Ingress/egress ring buffers in Cluster or Shared Memory
  - Classify ingress packet/cell, DMA to ring buffer
  - Assemble egress packets from chained DMA buffers
  - Ring buffer synchronization

# Efficiency for low power

---

- **Scalable multi-processor parallelism**
  - Many small DSPs exploit channel task parallelism
  - Higher efficiency than fewer large VLIW DSPs
- **Shared program memory**
  - Significant reduction in area and power vs. DSP farms
  - Instruction caches reduce memory demand
- **Cluster memory shared by DSPs and CP**
  - Enables scalable DSP array, pool scheduling
  - Vector DSPs reduce memory demand
- **Avoid task preemption, minimize overhead**
  - No cycles wasted on DSP task preemption
- **Balanced DSP/RISC MCPS and memory**
  - Channel density typically limited equally

# Calisto™ BCM1510 Implementation

---

- **Implementation**

- 130 M transistors
- .13μm CMOS -G
- 166 MHz clock
- 1.2 V core, 2.5 V I/O
- **1.2 Watts**
- 239 BGA 19x19 mm
- Q1/2002 production



- **Low power design**

- Extensive clock gating
- Low power pipelined busses

- **RAM defect repair**

- Redundant rows and columns
- Manufacturing test, laser repair

- **16 SpiceEngine DSPs**

- 2.7 GIPS
- 2.7 GMACS, 26.6 GOPS
- 16 KB Vector registers
- 18 KB Cache

- **5 RISC Processors**

- 830 MIPS
- 40 KB Cache

- **768 KB Shared Memory**

- 10.6 GB/sec bandwidth

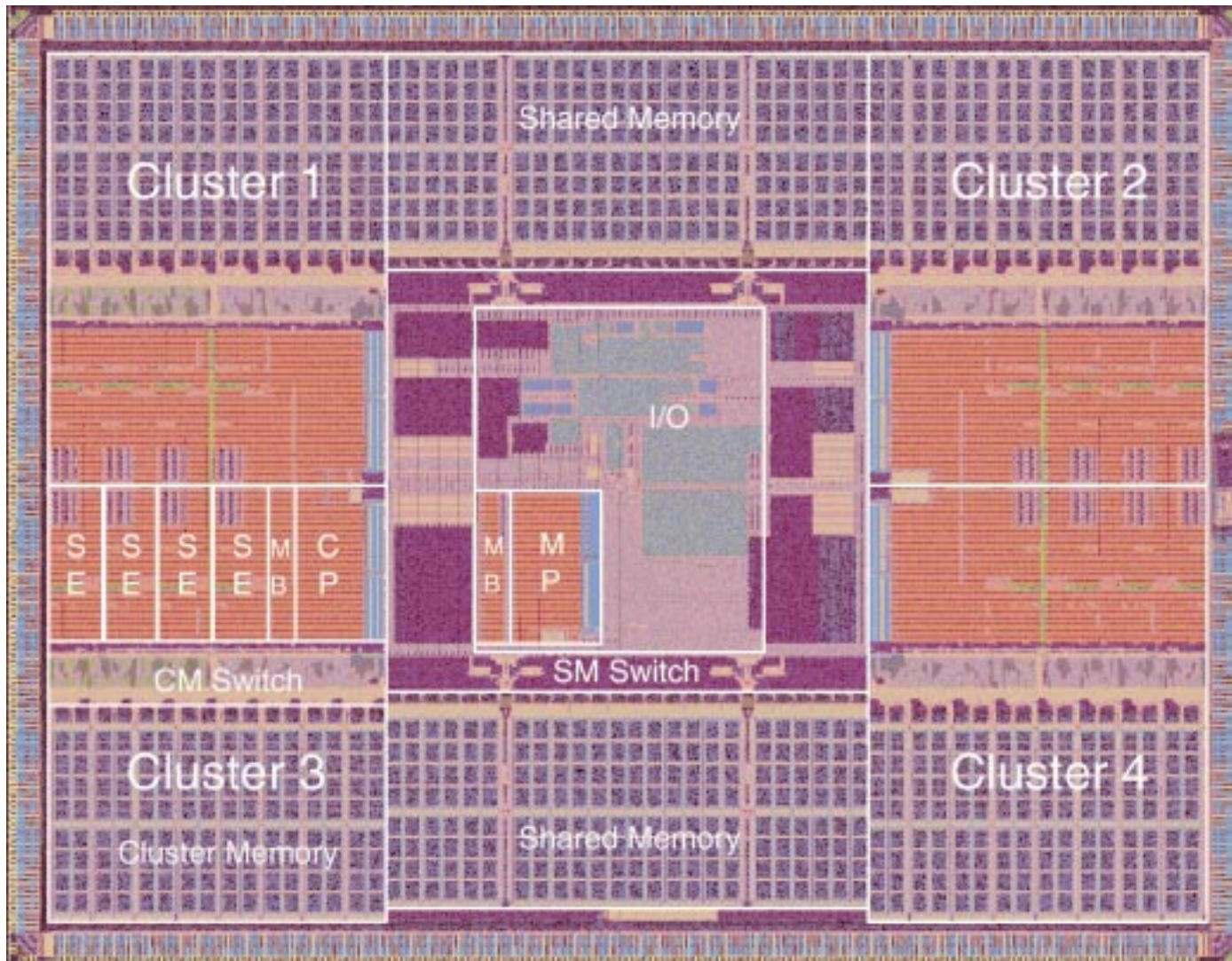
- **1 MB Cluster Memory**

- 18.6 GB/sec bandwidth

- **Multi-channel I/O**



# Calisto™ BCM1510



# OS Low Latency Scheduling

---

- **Multi-channel real-time OS**
  - Develop application service stack for single channel
  - OS maps each channel to a periodic per-frame channel task
  - OS/MMU restricts tasks to access only assigned channel memory
- **Schedule per-frame channel tasks in a periodic window**
  - Combine up/down, DSP/packet processing in one per-frame task
  - Run each per-frame task to completion, within known deadline
  - Zero cycles wasted on SE task preemption
- **OS schedule minimizes longest processing latency**
  - Stagger channel tasks relative to input frames, schedule output
  - Highest priority task gets next available SpiceEngine
    - Achieves less than 250  $\mu$ sec output packet jitter
- **OS distributed across clusters**
  - Each CP manages its cluster resources

# BCM1510 Gateway Performance

---

- **Calisto Gateway xChange™ software**



- Complete carrier-class VoP gateway service suite
- ITU bit-exact vocoders, G.7xx, GSM, BroadVoice, ...
- 64/128 msec adaptive line echo cancellation (ECAN)
- Voice activity detection, comfort noise generation
- DTMF tone detect/generate, tone relay, fax/modem detect
- Fax relay, Fax modems, T.38 FoIP, AAL2 Annex M
- Packet interface: IP/RTP/UDP, ATM AAL1/2/5, adaptive jitter buffer
- Conference mixing, in-band signaling, remote test, encryption

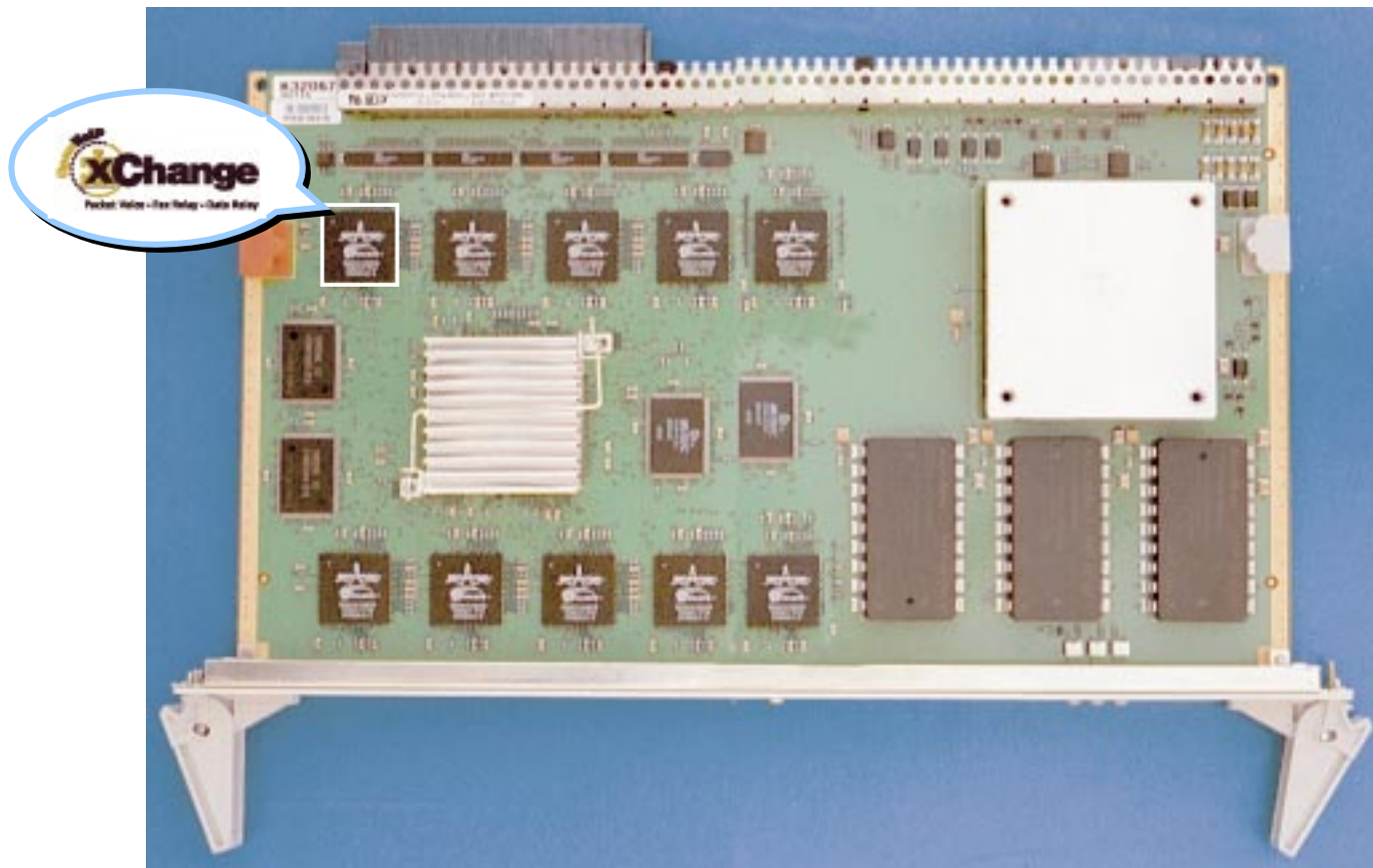
- **Breakthrough density for VoP Gateways**

- 240/220 channels G.711 VoP, 32/64 msec ECAN, **5 mW/channel**
- 184 channels G.711 VoP, 128 msec ECAN
- 120 channels G.729a VoP, 64 msec ECAN
- 104 channels G.729ab VoP, 128 msec ECAN, T.38 Fax relay
- Enables 2,016 channel OC-3 gateway blade with 10 chips



# Calisto™ OC-3 Gateway Blade

- Simple array of 10 Calisto™ BCM1510 chips
- Carrier-class multi-service Gateway xChange™ software
- ➔ Enables 2,016 channel OC-3 packet voice gateway blade



# Calisto™ Summary

---

- **Multi-channel multi-service communications platform**
  - Integrated multi-processor system
  - Balanced performance and memory
  - Consistent real-time performance
  - Flexible C programmable platform
- **Efficient low-power architecture**
  - Appropriate use of parallelism
  - Shared resources
  - Vector DSPs reduce memory usage
  - Low power design and implementation
- **Tightly coupled OS and software**
  - Enables carrier-class gateways



## Calisto™ BCM1510:

- 16 SpiceEngine DSPs
- 5 Control Processors
- Multi-channel I/O
- 1.75 MB Memory
- .13μm CMOS
- 166 MHz
- 1.2V, 1.2 Watts
- 239 BGA 19x19 mm
- Q1/2002 production